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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,932	04/12/2004	Masao Murade	119271	2127
25944 7590 05/16/2007 OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER MA, CALVIN	
			ART UNIT 2609	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/821,932	Applicant(s) MURADE, MASAO	
	Examiner Calvin Ma	Art Unit 2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The references listed on the Information Disclosure Statement filed on April 12, 2004 and January 10, 2006 have been considered by examiner; see attached PTO-1449.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an

Art Unit: 2609

invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-12 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-21 of U.S. Application No. 10/826,362. Although the conflicting claims are not identical, they are not patentably distinct from each other for the reason below.

Claims 1, 13, and 16 of the application No. 10/826,362.	Claim 1 of the application 10/821932
(Claim 1) An electro-optic device, comprising: a substrate; data lines extending in one direction above the substrate; scanning lines extending in a direction orthogonal to the data lines above the substrate; the switching elements being disposed above the substrate; pixel electrodes to which image signals are supplied from the data lines through the switching elements, the substrate having an image display area including the pixel electrodes and the switching elements, and a peripheral area at a periphery of an image display area;	An electro-optical device comprising: a substrate; data lines formed above the substrate and extending in a predetermined direction and scanning lines formed above the substrate and extending in a direction intersecting the data lines; switching elements to which scanning signals are supplied from the scanning lines; pixel electrodes to which image signals are supplied from the data lines via the switching elements; an image display region defined as a region of the substrate in which the pixel electrodes and the switching elements are formed; a peripheral region defining the periphery of the image display region;

<p>(Claim 1) storage capacitors that hold an electrical potential at the pixel electrodes for a predetermined time, the storage capacitors being disposed above the image display area; first wiring that supplies capacitor electrodes of the storage capacitors with a predetermined electrical potential, the first wiring being disposed above the image display area; and a frame formed as the same film as the first wiring, the frame being disposed at at least a part of a frame area between the image display area and the peripheral area.</p>	<p>exterior circuit connection terminals provided above the peripheral region along a peripheral side of the substrate; storage capacitors provided above the image display region to retain potentials of the pixel electrodes for a predetermined period of time; and a capacitor wire which supplies a predetermined potential to capacitor electrodes forming the storage capacitors and which is formed as the same film as that for electrodes forming the exterior circuit connection terminals.</p>
<p>(Claim 13) external circuit-connecting terminals disposed along an edge of the substrate, the external circuit-connecting terminals being disposed above the peripheral area;</p>	
<p>(Claim 16) The electro-optic device according to claim 13, the first wiring not being electrically coupled with the frame, a first portion of the second wiring being electrically coupled with the first wiring, a second portion of the second wiring being electrically coupled with the frame, the first portion being connected with a first portion of the external circuit-connecting terminals, and the second portion being connected with a second portion of the external circuit-connecting terminals.</p>	

Note the comparison above; claim 1 of the instant application is not patentably distinct from claims 1, 13, and 16 of U.S.P.G Pub.2004/024551. For example, claim 1 of the application is broader than claims 1, 13 and 16 of the U.S. Application 10/826362 by removing the limitation "first and second wiring." Thus, it would have been obvious to one of ordinary skill in the art at the time the

Art Unit: 2609

invention was made to have removed the limitation "first and second wiring" from claims 1, 13, and 16 of application No. 10/826,362 where that functionality is not needed.

Claims 2-12 are rejected to as being dependent upon a rejected base claim 1. Moreover, dependent claims 2-12 are recited the same limitation as dependent claims in the application No. 10/826,362.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7, 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurashina (U.S. Patent 6,597,413).

As to claim 1, Kurashina discloses an electro-optical device (see Fig. 1) comprising:

a substrate (i.e. TFT array substrate 10) (see Fig. 3, Col. 15, Line 8);

data lines (6a) formed above the substrate (10) and extending in a predetermined direction (i.e. the data line are arrangement orthogonally and there for has a predetermined vertically aligned direction) (see Fig. 6) and

Art Unit: 2609

scanning lines (3a) formed above the substrate (10) and extending in a direction (i.e. being perpendicular to the data line) (see Fig. 6) intersecting the data lines (i.e. the data lines 6a and scanning lines 3a are clearly intersecting and above the substrate 10) (see Fig. 6, Fig. 7, Col. 19, Lines 63-67, Col. 20, Lines 1-23);

switching elements (i.e. switching TFT 30) to which scanning signals (G1,G2,..Gn) are supplied from the scanning lines (3a) (see Fig. 6-10, Col. 19, Lines 25-36);

pixel electrodes (9a) to which image signals(S1, S2, .. Sn) are supplied from the data lines (6a) via the switching elements (30) (i.e. the TFT clearly is connected to the data line and the pixel electrode) (see Fig. 7, Col. 19, Lines 16-29);

an image display region (i.e. the actual displaying area of the display with respect to the substrate) defined as a region of the substrate (10) in which the pixel electrodes (9a) and the switching elements (30) are formed (i.e. the image display area is where the TFT 30 and the pixel electrode 9a reside) (see Fig. 7, Col. 19, Lines 50-53);

a peripheral region (i.e. area surrounding the display area) defining the periphery of the image display region (area of 9a and 30) (see Fig 7, Col. 19, Lines 50-53);

exterior circuit connection terminals (3a) (i.e. since the scanning line travels to the exterior of the immediate circuit, it is a exterior circuit connection terminal) (see Fig. 1) provided above the peripheral region along a peripheral side of the substrate (i.e. area immediately surrounding 30 and 9a) (see Fig. 7).

storage capacitors (70) provided above the image display region to retain potentials of the pixel electrodes (9a) for a predetermined period of time (i.e. since the storage capacitor 70 overlaps the pixel electrode 9a it is in the image display region) (see Fig. 7, Col. 20, Lines 1-23);

and a capacitor wire (i.e. capacitive line, 11a) which supplies a predetermined potential to capacitor electrodes forming the storage capacitors (70) (see Fig. 7, Col. 19, Lines 50-63) and which is formed as the same film as that for electrodes forming the exterior circuit connection terminals (i.e. the capacitor wire is fabricated on the same conductive layer as the scanning lines 3a) (see Fig. 1, Col. 1, Lines 37-40).

As to claim 2, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire (11a) formed on the data lines (6a) with a first interlayer insulating film (12) interposed therebetween (see Fig. 7, Col. 19, Lines 50-63).

As to claim 3, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire (11a) formed in a layer located immediately under a layer including the pixel electrodes (9a) (i.e. the capacitor wire 11 is clearly formed under the pixel electrode 9a) (see Fig. 7, Col. 19, Lines 50-63).

Art Unit: 2609

As to claim 4, Kurashina teaches the electro-optical device according to claim 1, the capacitor electrodes (70-3) provided below the data lines (6a) with a second interlayer insulating film (312) interposed there between (i.e. the capacitor electrode (i.e. part of the capacitor 70-3 is clearly formed under the pixel electrode 6a with insulating film 311 in between) (see Fig. 7, Col. 19, Lines 63-67, Col. 20, Lines 1-23).

As to claim 5, Kurashina teaches the electro-optical device according to claim 1, further comprising: a scanning line drive circuit (104), a potential supplied to the capacitor wire (11a) including a potential supplied to the scanning line drive circuit (i.e. it is inherent that since the scanning line is directly connected to the capacitor wire 11a that the potential supplied are from the scanning line drive circuit (104) (see Fig. 7, Fig. 42, Col. 37, Lines 41-55).

As to claim 6, Kurashina teaches the electro-optical device according to claim 1, further comprising: a counter substrate (20) and a counter electrode (21) provided above the counter substrate (20) (see Fig. 3, Col. 15, Lines 21-25);

a potential supplied to the capacitor wire including a potential supplied to the counter electrode (it is inherent that in order to form a working LCD cell shown in Fig. 42, the two electrodes that exist on the two substrates forming the cell uses the same power inputted from the external electrode (102) as the

Art Unit: 2609

capacitor line 11a in Fig. 7, which describe one possible lay out of the LCD cell design) (see Fig. 7, Fig. 41, Fig. 42, Col. 15, Lines 6-26, Col.37, Lines 41-67).

As to claim 7, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire including a shading material (11a light shielding film) (i.e. the first light shielding film 11a also serving as capacitive line) (see Fig. 7, Col. 19, Lines 50-53).

As to claim 9, Kurashina teaches the electro-optical device according to claim 1, the capacitor wire having a lattice pattern in the image display region when viewed in plan (i.e. the capacitor wire 11a in the clearly has a regular repeating grid pattern that resemble a lattice) (see Fig. 23, Col. 28, Lines 23-36).

Claim 12 is rejected on the same ground as claim 1, since the same limitation is cited.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

Art Unit: 2609

obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina in view of Kim (U.S.P.G. Pub 2006/0102903).

As to claim 8, Kurashina teaches the electro-optical device according to claim 1 but does teach the capacitor wire having a multilayer structure including different materials. Kim teaches the capacitor wire (25) having a multilayer structure including different materials (i.e. the storage electrode line 25 have double-layer or triple layer structure for instance Cr/Al or Al alloy, or Al alloy/Mo may be used) (see Fig. 19, Col. 12, Line 16 - Col. 13, Line 6) Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the capacitor lines of Kurashina with Kim's design with multiple layers with different materials in order to prevent non-uniformity in the display due to difference in parasitic capacitance (Col. 1, Lines 50-67, Kim).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina in view of Matsushima et al. (U.S.P.G. Pub 2003/0202800).

As to claim 10, Kurashina teaches the electro-optical device according to claim 9, the capacitor wire formed in the lattice pattern, but does not teach having intersections each having at least one of approximately triangle shaped section

Art Unit: 2609

at least one of four corners of the intersections. Matsushima teaches having intersections each having at least one of approximately triangle shaped section (112) (i.e. triangular conductor) at least one of four corners of the intersections. (i.e. by providing a triangular conductor on the inner angular portion thereof and further restrains capacitance from fluctuating between the inner angular portion of the signal wiring conductor) (see Fig. 3, [0052])

Therefore it would be obvious for one skill in the art at the time of the invention to have modified the capacitor wire of Kurashina with the angular design of Matsushima in order to restrain capacitance from fluctuation (see [0052], Matsushima).

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashina in view of Murade (US Patent 6,480,244).

As to claim 11, Kurashina teaches the electro-optical device according to claim 1, but does not teach a step-adjusting film under a region corresponding to the exterior circuit connection terminals, the step-adjusting film adjusting the height of the capacitor wire and that of the exterior circuit connection terminals to be approximately equivalent to each other with respect to the surface of the substrate.

Murade, teaches step-adjusting film under a region corresponding to the exterior circuit connection terminals, the step-adjusting film adjusting the height of the capacitor wire and that of the exterior circuit connection terminals to be approximately equivalent to each other with respect to the surface of the substrate (i.e. adjusting the film thickness of the lift-up film to be approximately equal to that of the exterior circuit connection terminals (scanning line) and capacitor line) (see Col. 3, Lines 51-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the step adjustment capability of Murade's design to the display control circuit layout of Kurashina to avoid decreasing in process yield, when pixels are made fine (see Col. 2, Lines 43-52, Murade).

Conclusion

The examiner also found several points of similarity between the present application and another by the inventor (U.S.P.G. Pub: 2004/0017628). Kim (U.S.P.G. Pub: 2004/0102903) is additionally cited to teach a multi-layer capacitor wire.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Calvin Ma whose telephone number is


Art Unit: 2609

(571)270-1713. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571)272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
May 10, 2007


CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER